Quarterly Progress Report

(April 1, 1993 through June 30, 1993)

on

VLSI for High-Speed Digital Signal Processing

prepared for

Office of Naval Research
800 North Quincy Street
Arlington, VA 22217-5000

Scientific Officer: Dr. Clifford Lau

Grant No.: N00014-91-J-1852
R & T Project: 4148503-01

Principal Investigator:

Alan N. Willson, Jr.
7400 Boelter Hall
University of California
Los Angeles, CA 90024-1600
(310)825-7400
e-mail: willson@ee.ucla.edu

VLSI for High-Speed Digital Signal Processing

Quarterly Progress Report - 4/1/93 through 6/30/93

Programmable Processor Ring Project

During the past quarter we have begun testing our single-processor ICs which we received from MOSIS. The chip provides for 11-bit input and output data with 16-bit internal data and 12-bit coefficients (stored in on-chip memory). The chip also has an 8-bit microprocessor bus interface for loading programs and coefficients. The IC contains 25,000 transistors and occupies an area of 14.8 mm^2 (3.7 mm by 4.0 mm including pads) in 1.2-μm CMOS technology. A block diagram of the chip is shown in Figure 1. Initial testing shows that the chip is fully functional. We are in the process of testing the performance and power dissipation of the chip and characterizing the input and output timing. From simulations we expect the chip to operate at 50 MHz.

We have also begun the layout of the final five-processor ring chip. This chip will be fabricated in Hewlett-Packard's 0.8 - μm CMOS process, through MOSIS. If our testing of the one-processor chip and our simulations of the five-processor layout can be completed by early September then we hope to have the chip included on the September 15 MOSIS run. It looks more likely, however, that we will not quite be ready by then, which means we will have to wait for the next 0.8 - μm run on January 5. Since this five-processor chip will be very large and its fabrication is expensive, we intend to take the time necessary to test and simulate thoroughly, thereby maximizing our chance for successful fabrication.

A circuit board that will use four ring processor chips is being designed and built to demonstrate the chip's capability of performing real-time video processing and high-speed one-dimensional processing of data. The circuit board will reside in an IBM-PC computer and will be accessed through the PC bus. A custom software package will be written which will both program the ring-processor chips with their instructions and filter coefficients and configure the circuit board for one of several different modes of operation. In the image processing case the board can either be configured to accept live NTSC video for real-time image processing or an image may be uploaded from the PC for benchmarking various filter masks. For one-dimensional filtering the board can be configured to accept high-speed digital data for real-time processing or data can be uploaded from the PC for non-real-time processing. A block diagram of the circuit board is shown in Figure 2.

Currently, the schematics for the circuit board have been completed and the building of the hardware has begun. The control logic for the board is being implemented with programmable logic devices. At this time most of the programs for these EPLD's have been written and simulated.

As the circuit board is being built, the software package is also being written and will serve as a diagnostics tool when testing the board. A working board utilizing these four ring-processors will be completed during the third quarter of 1993. This will coincide with the completion of a software package which will provide the user interface to the board.

A Programmable Digital Signal Processor Using Switchable Unit-Delays for Optimal Coefficient Allocation

The programmable FIR digital filter prototype chips discussed in the last report were all found capable of operating at data rates between 180 and 185 MHz. They therefore exceeded our target specification of 175 MHz. During this quarter UCLA has filed for a patent on this invention, and we have begun to receive a number of inquiries about the work from various commercial DSP establishments. We are presently in the process of writing an article for journal publication that describes the work.

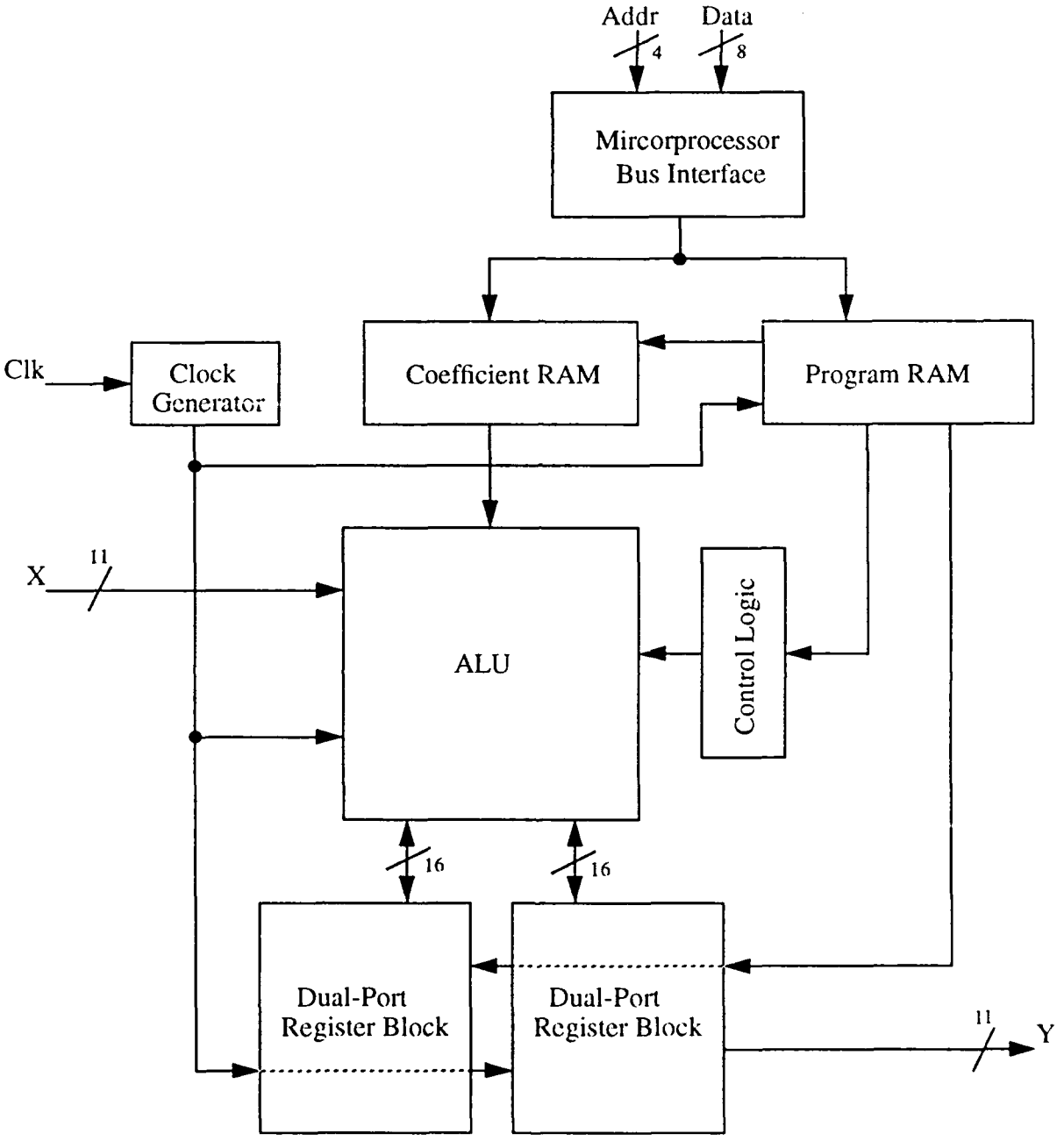

Figure 1 - Single-Processor IC Block Diagram

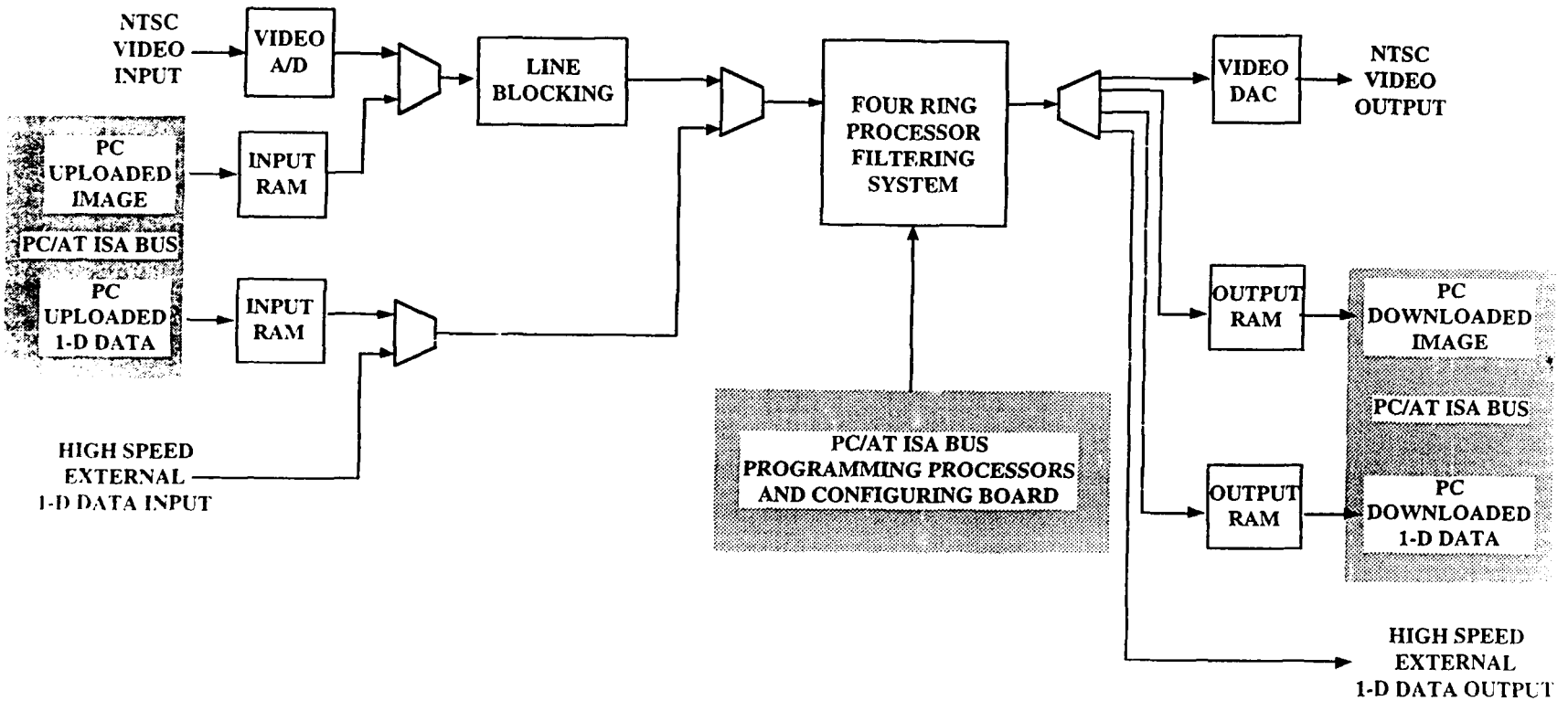

Figure 2 - Programmable Filter Processor Circuit Board